REMARKS

Claims 1-12 are pending in the Application.

Claims 1-12 stand rejected.

Applicant thanks the Examiner for discussing the present Office Action, and in particular, the claim objections, the rejections under 35 U.S.C. §112, and the rejections under 35 U.S.C. §102, with Applicant's attorney, on October 29, 2004.

I. OBJECTIONS TO THE DRAWINGS

The Examiner has objected to Figure 4B because the reference sign "03" should be "Ø3" as well as missing a label for elements 403A-E. The Examiner has further objected to Figure 4A since elements 401A-E do not contain a label. Applicant has amended Figure 4B to include the appropriate reference sign "Ø3" as well as added the label of "Flip-Flop" to elements 403A-E, as indicated above. Applicant, however, does not believe that a label to elements 401A-E is warranted as a person of ordinary skill in the art understands that the symbols of elements 401A-E are NAND gates.

The Examiner further objects to Figures 5A and 5B for not being discussed in the Specification. Applicant respectfully traverses. Applicant points out that Figures 5A and 5B were discussed as a single Figure 5 on pages 11-13 of the Specification. Applicant has amended the Specification to refer to Figure 5 as Figures 5A and 5B, as indicated above.

Further, the Examiner states that reference signs "Ø1B", Ø2B", Ø3B", Ø4B" and "Ø5B" are not mentioned in the Specification. Applicant respectfully traverses. Applicant respectfully directs the Examiner's attention to the paragraph beginning at line 25, page 10 and ending at line 17, page 11 where these reference signs are discussed. Applicant has also amended the Specification to add the reference signs "Ø1B", Ø2B", Ø3B", Ø4B" and "Ø5B" in the paragraph beginning at line 4, page 9.

II. OBJECTIONS TO THE SPECIFICATION:

The Examiner has objected to the Specification for not including the serial numbers of the referenced related applications. Applicant has amended the Specification to include the serial number of the referenced application.

The Examiner has further objected to the Specification to replace the term "illustrates" on page 5, line 11 of the Specification with the term "illustrate." Applicant has amended the Specification accordingly.

The Examiner has further objected to the Specification to replace the term "Figure 5" on page 11, line 21 of the Specification with the term "Figure 4A." Applicant has amended the Specification accordingly.

The Examiner has further objected to the Specification to replace the term "Claims" with the phrase "We claim." Applicant has amended the Specification accordingly.

III. CLAIM OBJECTIONS

The Examiner has objected to claims 1-12 for many informalities listed on page 4 of the present Office Action. Applicant has amended claims 1, 2, 4, 6, 7, 8, 9 and 10 as suggested by the Examiner.

IV. REJECTIONS UNDER 35 U.S.C. §102(b)

The Examiner has rejected claims 1-12 under 35 U.S.C. §102(b) as being anticipated by Tash et al. (U.S. Patent No. 5,127,023). Applicant respectfully traverses these rejections. For a claim to be anticipated under 35 U.S.C. §102, each and every claim limitation must be found within the cited prior art reference and arranged as required by the claim. M.P.E.P. §2131.

Applicant respectfully asserts that Tash does not disclose "an oscillator outputting three or more phases of a clock signal" as recited in claims 1 and 7. The Examiner cites column 7, lines 4-28 and element A2 as disclosing the above-cited claim limitation. Applicant respectfully traverses and asserts that Tash instead discloses a clock generation and control circuit that generate a pair of complementary clock signals, A2 and A2', as illustrated in Figure 4. There is no language in the cited passage that discloses three or more phases of a clock signal. Instead, the cited passage teaches outputting a signal and its complement. Neither is there any language in the cited passage that discloses an oscillator. Thus, Tash does not disclose all of the limitations of claims 1 and 7, and thus Tash does not anticipate claims 1 and 7.

Applicant further asserts that Tash does not disclose "a retiming mechanism coupled to said oscillator having circuitry for receiving said phases of said clock signal and serial data, and circuitry operable to reduce timing uncertainties in said serial data by outputting a value of said serial data sampled at a particular phase of said clock signal" as recited in claim 1 and similarly in claim 7. The Examiner cites column 7, lines 4-28 and 50-63, column 7, line 68 – column 8, line 4 and elements 74-76 and 82 of Tash as disclosing the above-cited claim limitations. Applicant respectfully traverses. As stated above, Tash instead discloses a clock generation and control circuit that generates a pair of complementary clock signals, A2 and A2', as illustrated in Figure 4. Tash further discloses that registers 74 and 75 serially shift the retimed bilevel data signals received by transceiver 52 through a window of time which is wide enough to detect the end of a data frame. Tash further discloses that when the first of shift registers 74 and 75 is entirely filled with high level signals, circuit 76 will activate a signal to indicate the end of the data frame. Tash further discloses that NAND gate 82 outputs a retimed and delayed positive-sense signal that was input to register 74.

There is no language in the cited passages that discloses phases of a clock signal as discussed above. Neither is there any language in the cited passages that discloses an oscillator for outputting phases of a clock signal. Neither is there any language in the cited passages that discloses sampling a value of serial data at a particular phase of a clock signal. Thus, Tash does not disclose a retiming mechanism that receives phases of a clock signal and serial data. Further, Tash does not disclose reducing timing uncertainties in serial data by outputting a value of serial data sampled at a particular phase of the clock signal.

Further, Tash does not disclose "wherein said retiming mechanism comprises a plurality of first units, wherein each of said plurality of first units comprises circuitry for sampling said serial data using a particular phase of said clock signal" as recited in claim 2 and similarly in claim 8. Furthermore, Tash does not disclose "wherein each of said plurality of first units comprises circuitry for receiving said particular phase of said clock signal and a complement of said particular phase of said clock signal and said serial data" as recited in claim 3 and similarly in claim 9. The Examiner cites shift registers 74 and 75 of Tash as disclosing the above-cited claim limitations. Applicant respectfully traverses and asserts that shift registers 74 and 75 serially shift a data signal and its complement as well as receiving a clock signal, A2, and it complement, A2', as illustrated in Figure 4. Column 7, lines 8-12. However, there is no language in Tash that discloses that the shift registers sample serial data using a phase of a clock signal. Neither is there any language in Tash that discloses that the shift registers receive a phase of a clock signal and its complement. Thus, Tash does not disclose all of the limitations of claims 2-3 and 8-9, and thus Tash does not anticipate claims 2-3 and 8-9.

Applicant further asserts that Tash does not disclose "wherein said retiming mechanism further comprises a plurality of second units, wherein each of said plurality of second units is associated with a particular first unit, wherein each of said plurality of second units comprises circuitry for outputting the value of said serial

data sampled by said associated first unit upon activation" as recited in claim 4 and similarly in claim 10. The Examiner cites NAND gate 110 and NAND gate 113 of Tash as together operating as a second unit as well as NAND gate 111 and NAND gate 113 of Tash as together operating as a second unit. The Examiner further cites the D flip-flops of shift registers 74 and 75 of Tash as disclosing a first unit. Applicant respectfully traverses that Tash discloses the above-cited claim limitations.

Tash instead discloses that each flip-flop in a shift register (element 74 or 75) is coupled to NAND gate 110 which is coupled to NAND gate 113. Since only one NAND gate, NAND gate 110, is coupled to each flip-flop in the shift register, which the Examiner cites as disclosing a first unit, Tash does not disclose that each second unit is associated with a particular first unit. That is, Tash does not disclose having multiple NAND gates 110 where each of these NAND gates 110 is associated with a particular flip-flop.

Furthermore, Tash discloses that a RESET signal is activated when the first of shift registers 74 and 75 is entirely filled with high-level signals. Column 7, lines 55-57. Tash further discloses that NAND gate 113 outputs signal A6 which corresponds to the RESET signal as illustrated in Figure 6. However, there is no language in Tash that discloses that the RESET signal corresponds to a value sampled by a flip-flop upon activation of the second unit, which the Examiner asserts corresponds to NAND gate 110/111 in combination with NAND gate 113. Thus, Tash does not disclose a second unit outputting the value of a serial data sampled by an associated first unit upon activation. Further, Tash does not disclose all of the limitations of claims 4 and 10, and thus Tash does not anticipate claims 4 and 10.

Applicant further asserts that Tash does not disclose "wherein a particular second unit of said plurality of second units is activated based on a logical state of each input to said particular second unit" as recited in claim 5 and similarly in claim 11. Applicant further asserts that Tash does not disclose "wherein said logical state of

each input is determined based on combinational logic using said phases of said clock signal and complements of said phases of said clock signal" as recited in claim 6 and similarly in claim 12. The Examiner has not cited any passage or element in Tash as disclosing these limitations. Accordingly, the Examiner has not presented a reference that discloses each and every claim limitation in claims 5, 6, 11 and 12. Thus, the Examiner has not presented a *prima facie* case of anticipation in rejecting claims 5, 6, 11 and 12.

The Examiner has rejected claims 1-12 under 35 U.S.C. §102(b) as being anticipated by Jung et al. (U.S. Patent No. 5,887,040). Applicant respectfully traverses these rejections.

For a claim to be anticipated under 35 U.S.C. §102, each and every claim limitation must be found within the cited prior art reference and arranged as required by the claim.

Applicant asserts that Jung does not disclose "a retiming mechanism coupled to said oscillator having circuitry for receiving said phases of said clock signal and serial data, and circuitry operable to reduce timing uncertainties in said serial data by outputting a value of said serial data sampled at a particular phase of said clock signal" as recited in claim 1 and similarly in claim 7. The Examiner asserts that element 202 of Jung discloses the retiming mechanism as claimed. Applicant respectfully traverses. Jung instead discloses that element 202 receives multi-phase clock pulses and serial data to generate control signals for selecting one or more clock pulses. Column 3, lines 42-47. Generating control signals for selecting one or more clock pulses is not the same as outputting a value of a serial data sampled at a particular phase of the clock signal. Furthermore, there is no language in Jung that element 202 is coupled to an oscillator. Neither is there any language in Jung that element 202 is coupled to an oscillator that outputs phases of a clock signal. Neither is there any language in Jung that element 202 reduces timing uncertainties in the

serial data. Thus, Jung does not disclose all of the limitations of claims 1 and 7, and thus Jung does not anticipate claims 1 and 7.

Jung does not disclose "wherein said retiming mechanism comprises a plurality of first units, wherein each of said plurality of first units comprises circuitry for sampling said serial data using a particular phase of said clock signal" as recited in claims 2 and 8. Furthermore, Jung does not disclose "wherein each of said plurality of first units comprises circuitry for receiving said particular phase of said clock signal and a complement of said particular phase of said clock signal and said serial data" as recited in claims 3 and 9. The Examiner cites to element 203 of Jung as including a plurality of logic gates, as illustrated in Figure 10, which allegedly correspond to the first units as claimed. Paper No. 3, page 8. Applicant respectfully traverses the assertion that Jung discloses the above-cited claim limitations. Jung instead discloses that element 203 receives the multi-phase clock pulse and the retiming clock pulse select signals from element 202. Column 3, lines 53-56. Therefore, element 203 does not correspond to a retiming mechanism that receives phases of a clock signal and serial data, as required by claims 1 and 7. Instead, element 203 receives retiming clock pulse select signals and the multi-phase clock pulse. Furthermore, as illustrated in Figure 10, the OR gates of element 203 are receiving multi-phase delaying clocks. Column 7, lines 52-55. The OR gates of element 203, as illustrated in Figure 10, receive clock selecting signals from element 202. Column 7, lines 55-58. The OR gates of element 203 are not sampling serial data. Neither are the OR gates of element 203 sampling serial data using a phase of a clock signal. Further, the OR gates of element 203 do not receive a phase of a clock signal and its complement along with serial data. Thus, Jung does not disclose all of the limitations of claims 2-3 and 8-9, and thus Jung does not anticipate claims 2-3 and 8-9.

Applicant further asserts that Jung does not disclose "wherein said retiming mechanism further comprises a plurality of second units, wherein each of said

plurality of second units is associated with a particular first unit, wherein each of said plurality of second units comprises circuitry for outputting the value of said serial data sampled by said associated first unit upon activation" as recited in claim 4 and similarly in claim 10. The Examiner makes the blanket statement that all the logic circuits in Figures 6 and 7 correspond to second units. Applicant respectfully traverses that Jung discloses the above-cited claim limitations.

Jung instead discloses that Figures 6 and 7 illustrate an example of element 202 which, as discussed above, did not output a value of the serial data sampled at a particular phase of the clock signal, as required for a retiming mechanism as recited in claims 1 and 7. Further, each logic circuit in element 202 is not associated with the OR gate of element 203 which the Examiner has previously cited as disclosing a first unit. Further, none of the logic circuits in element 202, as illustrated in Figures 6 and 7, output a value of a serial data sampled by an OR gate of element 203 upon activation. Thus, Jung does not disclose all of the limitations of claims 4 and 10, and thus Jung does not anticipate claims 4 and 10.

Applicant further asserts that Jung does not disclose "wherein a particular second unit of said plurality of second units is activated based on a logical state of each input to said particular second unit" as recited in claim 5 and similarly in claim 11. Applicant further asserts that Jung does not disclose "wherein said logical state of each input is determined based on combinational logic using said phases of said clock signal and complements of said phases of said clock signal" as recited in claim 6 and similarly in claim 12. The Examiner makes the blanket statement that all the logic circuits in Figures 6 and 7 correspond to second units. Applicant respectfully traverses that Jung discloses the above-cited claim limitations.

The Examiner has not cited to any logic unit in Figure 6 or 7 that is activated based on a logical state of each input to the logic unit. Neither has the Examiner cited to any logic unit in Figure 6 or 7 where the logical state of each input to a logic unit is

determined based on combinational logic using the phases of the clock signal and complements of the phases of the clock signal. Thus, Jung does not disclose all of the limitations of claims 5, 6, 11 and 12, and thus Jung does not anticipate claims 5, 6, 11 and 12.

As a result of the foregoing, Applicant respectfully asserts that not each and every claim limitation was found within Jung, and thus claims 1-12 are not anticipated by Jung.

VI. CONCLUSION

As a result of the foregoing, it is asserted by Applicant that claims 1-12 in the Application are in condition for allowance, and Applicant respectfully requests an allowance of such claims. Applicant respectfully requests that the Examiner call Applicant's attorney at the below listed number if the Examiner believes that such a discussion would be helpful in resolving any remaining issues.

Respectfully submitted,

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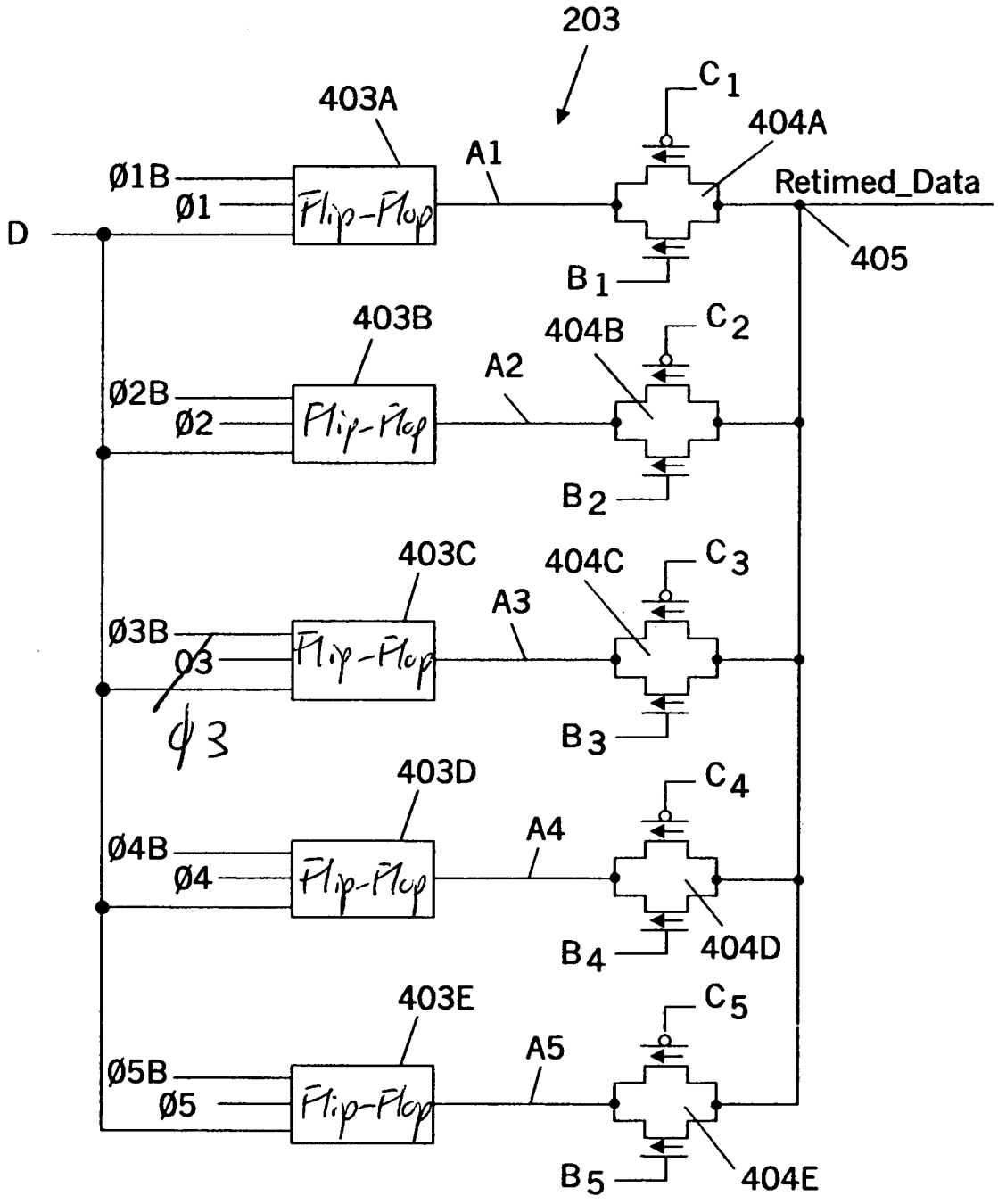
Serial No. 09/820,507
Amendment to Office Action of 8/16/2004
Annotated Sheet Showing Changes

FIG. 4B



IN THE DRAWINGS

Applicant has replaced the incorrect label "03" with the correct label "Ø3" in Figure 4B. Applicant has further added the label of "Flip-Flop" to elements 403A-E in Figure 4B. Applicant has attached an annotated sheet of Figure 4B indicating the replacement of the label "03" with the label "Ø3" as well as the addition of the label "Flip-Flop" to elements 403A-E. Applicant has further attached a replacement sheet for Figure 4B incorporating the changes mentioned above.

Attachment: Replacement Sheet
Annotated Sheet Showing Changes